

Notice of Allowability

Application No.

10/862,375

Examiner

Stephen Elmore

Applicant(s)

WARE ET AL.

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed December 13, 2004.
2. ☒ The allowed claim(s) is/are 33-90 renumbered as 1-58.
3. ☒ The drawings filed on 08 June 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.


Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 9-8-2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.


Stephen Elmore 1-21-2005
Primary Examiner
Art Unit 2186

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

In independent claims 33, 38, 43, 44, 49, 54, 55, 62, 66, 67, 75, 83, 84, 87 and 90, directed towards a memory system, and a method of operation in a memory system, the following limitations, taken in combination with the remaining features of the independent claims, are not found in and or are not obvious in view of the prior art of record:

Claims 33, 38, and 43,

"a second mode wherein both the first portion and the second portion of the memory core are accessible through the first set of interface connections";

Claims 44, 49, and 54,

"a second mode wherein both the first group and the second group of memory storage locations are accessible through the first set of interface connections";

Claim 55,

"a third memory storage location in the first memory module may be accessed through the first set of interface connections simultaneously while a fourth memory storage location in the third memory module is accessed through the third set of interface connections";

Claim 62,

"simultaneously accessing a third memory storage location in the first memory module through the first set of interface connections and a fourth memory storage location in the third memory module through a third set of interface connections, the third memory location and the fourth memory location being part of the second group of memory storage locations";

Claim 66,

"means for simultaneously accessing a third memory storage location in the first memory module through the first set of interface connections and a fourth memory storage location in the

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third memory module through a third set of interface connections, the third memory location and the fourth memory location being part of the second group of memory storage locations";

Claim 67,

"memory access circuitry for controlling access to the first and second memory modules through the first and second sets of interface connections, respectively, such that memory storage locations in the first and second memory modules may be accessed either independently or jointly through the first and second sets of interface connections, respectively, based upon the unique addresses of the memory storage locations";

Claim 75,

"accessing the plurality of memory modules in response to the request such that memory storage locations in a first of the plurality of memory modules and a second of the plurality of memory modules are accessed either independently or jointly through a first set of interface connections and a second set of interface connections, respectively, based upon the unique addresses of the memory storage locations";

Claim 83,

"means for accessing the plurality of memory modules in response to the request such that memory storage locations in a first of the plurality of memory modules and a second of the plurality of memory modules are accessed either independently or jointly through a first set of interface connections and a second set of interface connections, respectively, based upon the unique addresses of the memory storage locations";

Claims 84, 87, and 90,

"a second mode wherein both the first portion and the second portion of the single memory core are accessible through the first set of interface connections".

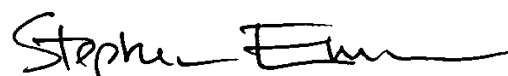
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2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Elmore whose telephone number is (571) 272-4436. The examiner can normally be reached on Mon-Fri from 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Stephen Elmore
Primary Examiner
Art Unit 2186

January 21, 2005